

# Chapter #9: Finite State Machine Optimization

# Chapter Finite State Machine Optimization

**Feng Gao**



## **Chapter Finite State Machine Optimization:**

*Finite State Machine Logic Synthesis for Complex Programmable Logic Devices* Robert Czerwinski, Dariusz Kania, 2013-01-12 This book is a monograph devoted to logic synthesis and optimization for CPLDs. CPLDs macrocell can also be interpreted as programmable AND fixed OR structure well known as PAL based structure. The question is what should be done when the number of implicants representing function exceeds the number of product terms available in a logic block. The answer is in the book. Logic synthesis and optimization methods dedicated for PAL based structures are proposed. The methods strive to find the optimum fit for the combinational logic and finite state machines to the structure of the logic device and aim at area and speed optimization. The theoretical background and complete strategies are richly illustrated with examples and figures.

*Logic Synthesis for FSM-Based Control Units* Alexander Barkalov, Larysa Titarenko, 2009-11-25 This book presents the hardware implementation of control algorithms represented by graph schemes of algorithm. It includes new methods of logic synthesis and optimization for logic circuits of Mealy and Moore FSMs oriented on both ASIC and FPLD.

***Logic Synthesis for FPGA-Based Mealy Finite State Machines*** Alexander Barkalov, Larysa Titarenko, Kazimierz Krzywicki, 2024-12-04 This book is devoted to the logic synthesis of field programmable gate array (FPGA) based circuits of Mealy finite state machines (FSM). Three new methods of state assignment are proposed which allow obtaining FSM circuits required minimum amount of internal chip resources. *Logic Synthesis for FPGA Based Mealy Finite State Machines: Structural Decomposition in Logic Design* contains several original synthesis and optimization methods based on the structural decomposition of FPGA based FSM circuits developed by the authors. To optimize FSM circuits the authors introduce the use of three methods of state assignment: twofold extended and composite. These methods allow for the creation of two or three level architectures of FSM circuits. The authors also demonstrate how the proposed methods, FSM architectures and synthesis methods can replace known solutions based on either functional decomposition or classical methods of structural decomposition. The authors also show how these architectures have regular systems of interconnections and demonstrate positive features compared to methods based on functional decomposition including producing circuits with fewer elements that are faster and consume less power than their counterparts. The book includes experimental results proving the efficiency of the proposed solutions and compares the numbers in Look up Tables (LUTs) showing the performance, maximum operating frequency and power consumption for various methods of state assignment. The audience for this book is students, researchers and engineers specializing in computer science, engineering, electronics and telecommunications. It will be especially useful for engineers working within the scope of algorithms, hardware based software accelerators and control units and systems based on the use of FPGAs.

*SystemVerilog for Hardware Description* Vaibbhav Taraate, 2020-06-10 This book introduces the reader to FPGA based design for RTL synthesis. It describes simple to complex RTL design scenarios using SystemVerilog. The book builds the story from basic fundamentals of FPGA based designs to advanced RTL design and

verification concepts using SystemVerilog It provides practical information on the issues in the RTL design and verification and how to overcome these It focuses on writing efficient RTL codes using SystemVerilog covers design for the Xilinx FPGAs and also includes implementable code examples The contents of this book cover improvement of design performance assertion based verification verification planning and architecture and system testing using FPGAs The book can be used for classroom teaching or as a supplement in lab work for undergraduate and graduate coursework as well as for professional development and training programs It will also be of interest to researchers and professionals interested in the RTL design for FPGA and ASIC

**Hardware for Soft Computing and Soft Computing for Hardware** Nadia Nedjah, Luiza de Macedo Mourelle, 2013-11-18 Single and Multi Objective Evolutionary Computation MOEA Genetic Algorithms GAs Artificial Neural Networks ANNs Fuzzy Controllers FCs Particle Swarm Optimization PSO and Ant colony Optimization ACO are becoming omnipresent in almost every intelligent system design Unfortunately the application of the majority of these techniques is complex and so requires a huge computational effort to yield useful and practical results Therefore dedicated hardware for evolutionary neural and fuzzy computation is a key issue for designers With the spread of reconfigurable hardware such as FPGAs digital as well as analog hardware implementations of such computation become cost effective The idea behind this book is to offer a variety of hardware designs for soft computing techniques that can be embedded in any final product Also to introduce the successful application of soft computing technique to solve many hard problems encountered during the design of embedded hardware designs Reconfigurable embedded designs for GAs ANNs FCs and PSO are presented and evaluated Also the application of quantum based evolutionary computation and multi objective evolutionary computation as well as ACO are applied to solve hard problems related to circuit synthesis IP assignment mapping and routing of applications on Network On Chip infrastructures

Formal Methods in VLSI System Design Adnan Aziz, 1996

Logic Synthesis for Finite State Machines Based on Linear Chains of States Alexander Barkalov, Larysa Titarenko, Jacek Bieganski, 2017-06-24 This book discusses Moore finite state machines FSMs implemented with field programmable gate arrays FPGAs including look up table LUT elements and embedded memory blocks EMBs To minimize the number of LUTs in FSM logic circuits the authors propose replacing a state register with a state counter They also put forward an approach allowing linear chains of states to be created which simplifies the system of input memory functions and therefore decreases the number of LUTs in the resulting FSM circuit The authors combine this approach with using EMBs to implement the system of output functions microoperations This allows a significant decrease in the number of LUTs as well as eliminating a lot of interconnections in the FSM logic circuit As a rule it also reduces the area occupied by the circuit and diminishes the resulting power dissipation This book is an interesting and valuable resource for students and postgraduates in the area of computer science as well as for designers of digital systems that included complex control units

**Finite State Machine Verification, Test, and Minimization** Sezer Gören, 2003

**Finite State Machine Datapath Design,**

**Optimization, and Implementation** Justin Davis, Justin S. Davis, Robert Bryan Reese, 2008 Finite State Machine Datapath Design Optimization and Implementation explores the design space of combined FSM Datapath implementations The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints and the use of pipelining for increasing system clock frequency This is followed by definitions for latency and throughput with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications Also design issues relating to functionality interfacing and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs single ports and dual ports are examined Selected design examples are presented in implementation neutral Verilog code and block diagrams with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms A working knowledge of Verilog logic synthesis and basic digital design techniques is required This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL

*Application-tuned Processor Architectures* Timothy Sherwood, 2003

*State Minimization of Finite State Machines Using Implicit Techniques* Timothy Yee-kwong Kam, 1995

**A Binary Decision Diagram Approach for Finite State Machine Encoding** Pi-Fuang Chen, 1997

Sequential Circuit Synthesis at the Gate Level Ellen Marie Sentovich, 1993

**On Efficient Software Realization of Sequential Machines** Yunjian Jiang, 2003

*A Synthesis System for Testable and Area-efficient Finite State Machines* Chun-Yeh Liu, 1994

*Computational Intelligence* Andries P. Engelbrecht, 2002 Computational Intelligence An Introduction offers an in depth exploration into the adaptive mechanisms that enable intelligent behaviour in complex and changing environments The main focus of this text is centred on the computational modelling of biological and natural intelligent systems encompassing swarm intelligence fuzzy systems artificial neural networks artificial immune systems and evolutionary computation Computational Intelligence An Introduction is essential reading for third and fourth year undergraduate and postgraduate students studying CI The first edition has been prescribed by a number of overseas universities and is thus a valuable teaching tool In addition it will also be a useful resource for researchers in Computational Intelligence and Artificial Intelligence as well as engineers statisticians operational researchers and bioinformaticians with an interest in applying AI or CI to solve problems in their domains

BOOK JACKET

**Gate-level Techniques for Low Power and Reliable Circuit Design** Feng Gao, 2005

U.S. Government Research & Development Reports, 1967

**The Harmonic Mind: Cognitive architecture** Paul Smolensky, Géraldine Legendre, 2006 An integrated connectionist symbolic architecture of the mind brain applied to neural genomic realisation of grammar acquisition processing and typology in phonology and syntax and foundations of cognitive explanation Despite their apparently divergent accounts of higher cognition cognitive theories based on neural computation and those employing symbolic computation can in fact strengthen one another To substantiate this controversial claim this landmark work develops in depth a cognitive architecture based in

neural computation but supporting formally explicit higher level symbolic descriptions including new grammar Illegible Detailed studies in both phonology and syntax provide arguments that these grammatical theories and their neural network realisations enable deeper explanations of early acquisition processing difficulty cross linguistic typology and the possibility of genomically Illegible universal principles of grammar Foundational questions concerning the explanatory status of symbols for central problems such as the unbounded productivity of higher cognition are also given proper treatment science through tutorial chapters and numerous expository boxes providing background material from several disciplines Examples common to different chapters facilitate the transition from more basic to more sophisticated treatments Details of method formalism and foundation are presented in later chapters offering a wealth of new results to specialists in psycholinguistics language acquisition theoretical linguistics computational linguistics computational neuroscience connectionist modelling and philosophy of mind

**Designing Effective Evolutionary Computations** Kumar Hemachandra Chellapilla, 2005

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