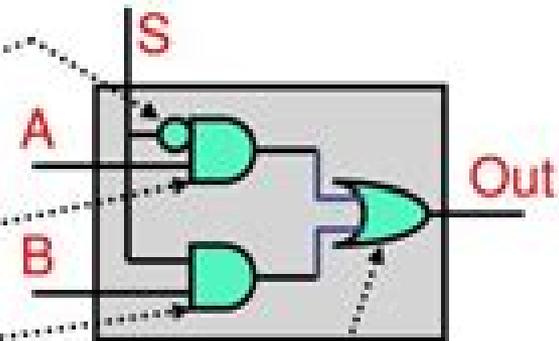


Verilog Structural vs Behavioral Example

Structural

```
module mux2to1(  
    input S, A, B,  
    output Out );  
    wire S_, AnS_, BnS;  
    not (S_, S);  
    and (AnS_, A, S_);  
    and (BnS, B, S);  
    or (Out, AnS_, BnS);  
endmodule
```



Behavioral

```
module mux2to1(  
    input S, A, B,  
    output Out );  
    assign Out = (~S & A) | (S & B);  
endmodule
```

Better:

```
assign Out = S? B:A;
```

32 Bit Multiplier Structural Verilog Code

Lingjun Ying



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